WHAT IS CLAIMED IS:

1. An integrated circuit (IC) chip comprising:

a square-wave audio signal generator adapted to generate square-wave signals at audio frequencies;

a counter adapted to digitally count from zero to a predetermined number;

a register adapted to hold a volume control value;

a comparator connected to said counter and connected to said register, said comparator adapted to compare the count with the volume control value and produce a modulation signal; and

an AND gate connected to said square-wave audio signal generator and connected to said comparator, said AND gate adapted to combine, in a logical AND operation, the audio frequency square-wave signal with the modulation signal.

2. The IC recited in Claim 1 wherein said square-wave audio signal generator generates a square-wave audio signal generator having a frequency within a range from 500 Hz to five KHz.

3. The IC recited in Claim 1 wherein said counter is a 5-bit counter adapted to count from 0 to 31.

4. The IC recited in Claim 1 wherein said counter operates at a counter frequency on the order of MHz.

5. The IC recited in Claim 1 wherein said register is a pulse width register having five bits.

6. The IC recited in Claim 1 wherein the integrated circuit chip is an application specific integrated circuit chip (ASIC).

7. A method of generating modulated square-wave audio signal, the method comprising:

generating a square-wave audio signal having a first audio frequency;

repeatedly counting a predetermined range of values generating count signals;

modulating the count signal with a volume control signal resulting in modulation signal; and

modulating the square-wave audio signal with the modulation signal.

8. The method recited in Claim 7 wherein the first audio frequency is within a range from 500 Hz to five KHz.

9. The method recited in Claim 7 wherein the digital counting step counts from 0 to 31.

10. The method recited in Claim 7 wherein the digital counting step operates a counter frequency on the order of MHz.

11. The method recited in Claim 7 wherein the volume control signal is set at a value within a range counted by the digital counting step.

12. An apparatus comprising:

an integrated circuit (IC) chip adapted to generate a

modulated audio frequency square-wave signal; and

an amplifier subsystem connected to said IC chip, the amplifier subsystem adapted to filter the modulated square-wave audio signal and to amplify the filtered audio signal.

13. The apparatus recited in Claim 12 wherein said IC chip comprises:

a square-wave audio signal generator adapted to generate square-wave signals at audio frequencies;

a counter adapted to digitally count from zero to a predetermined number;

a register adapted to hold a volume control value;

a comparator connected to said counter and connected to said register, said comparator adapted to compare the count with the volume control value and produce a modulation signal; and

an AND gate connected to said square-wave audio signal generator and connected to said comparator, said AND gate adapted to combine, in a logical AND operation, the audio frequency square-wave signal with the modulation signal.

14. The apparatus recited in Claim 13 wherein said square-wave audio signal generator generates a square-wave audio signal generator having a frequency within a range from 500 Hz to five KHz.

15. The apparatus recited in Claim 13 wherein said counter is a 5-bit counter adapted to count from 0 to 31.

16. The apparatus recited in Claim 13 wherein said counter operates at a counter frequency on the order of MHz.

17. The apparatus recited in Claim 13 wherein said register is a pulse width register having five bits.

18. The apparatus recited in Claim 13 wherein said amplifier subsystem comprises a resistor-capacitor (RC) filter connected to a fixed gain amplifier.